

15502

Roll No. _____

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15502

M. Tech. I - Sem. (Main) Exam., Dec. - 2018

VLSI Design

1MVL2 VLSI Design

Time: 3 Hours

Maximum Marks: 100

Min. Passing Marks: 33

Instructions to Candidates:

*Attempt any **five** questions, Marks of questions are indicated against each question. Draw neat and comprehensive sketches wherever necessary to clearly illustrate your answer. Assume missing data suitable if any and specify the same. Use of following supporting material is permitted during examination. (Mentioned in form No. 205)*

1. NIL

2. NIL

Q.1 (a) What is Voltage boot strapping? Explain briefly. [5]

(b) State the difference between ASIC and FPGA. [5]

(c) What are various implementation strategies for digital IC's? Explain in detail. [10]

Q.2 (a) Define the logical effort. [2]

(b) Consider a 5 mm long, 0.32 μm wide metal2 wire in a 180 nm process. The sheet resistance is $0.05\Omega/\square$ and capacitance is $0.2\text{ fF}/\mu\text{m}$. Construct a 3 – segment π -model for the wire. [8]

(c) Consider a process in which PMOS transistor have three times the effective resistance of nMOS transistor. A unit inverter with equal rising and falling delays

in this process is shown in Figure 1. Calculate the logical efforts of a 2 – input NAND gate and 2 – input NOR gate if they are designed with equal rising and falling delays. [10]

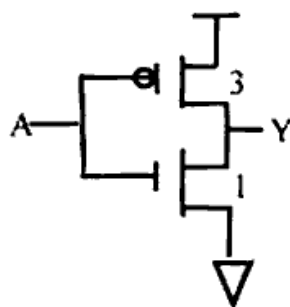


Figure - 1

Q.3 Draw the optimized layout of

(i) $Y = \bar{A}B + C\bar{D}E$ CMOS logic [10]

(ii) $Y = \overline{ABC + DEF}$ CMOS logic [10]

Q.4 (a) Define Clock Skew and Jitter. Explain the different mechanism to minimize in synchronous circuits. [10]

(b) A flip flop is built from a pair of transparent latches using non overlapping clocks. Express the set up time, hold up time and clock to Q delay of flip flop in terms of latches timing parameters and $t_{nonoverlap}$. [10]

Q.5 (a) Draw the basic cell architecture of - [10]

(i) Serial adder

(ii) Algorithmic shifter

(b) Estimate the minimum delay of 10:1024 decoder driving an electrical effort $H = 20$ using

(i) Static CMOS

(ii) Footless domino gates [10]

Q.6 (a) What is the need of sense amplifier in memories? Also draw its various forms and explain their operation. [10]

(b) (i) Determine the logic function F given in Figure – 2.

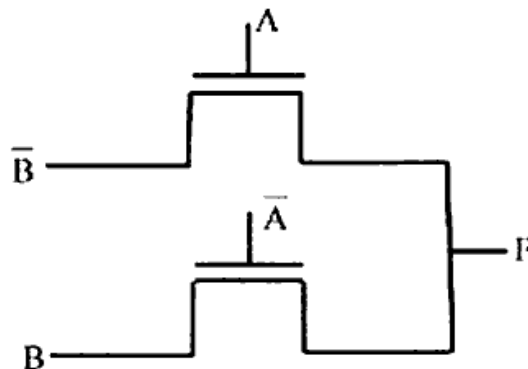


Figure-2

(ii) Design a circuit to implement the same logic function but using NOR gates. [10]

Q.7 (a) Design the Schmitt trigger using CMOS circuit. Also explain its working. [5]

(b) What is the metastability in digital circuits? How it can be avoided. [8]

(c) What are arbiters? Explain its operation also. [7]

Q.8 Write short note on the following: (Any two) [20]

(i) Barrel shifter

(ii) Power dissipation in memories

(iii) Testability and fault detection

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