

610501

Roll No: _____

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610501/610601

B. Tech. VI - Sem. (Main) Exam., (Academic Session 2021- 2022)

Electrical & Electronics Engineering

6EX3 – 01 Computer Architecture

Common with EEE & EE

Time: 2 Hours

Maximum Marks: 80

Min. Passing Marks:

Instructions to Candidates:

***Part – A: Short answer questions (up to 25 words) 2×3 marks = 6 marks.
Candidates have to answer two questions out of five.***

***Part – B: Analytical/Problem solving questions 3×15 marks = 45 marks.
Candidates have to answer three questions out of six.***

***Part – C: Descriptive/Analytical/Problem Solving questions 1×29 marks = 29 marks.
Candidates have to answer one questions out of three***

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

*Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)*

1. NIL

2. NIL

PART – A

Q.1 What is the instruction level parallelism?

Q.2 Define MIPS.

~~Q.3~~ State the advantages of virtual memory.

Q.4 Define VLIW.

~~Q.5~~ What are the components of a computer system?

PART – B

- Q.1 Discuss about the various component of a computer system.
- Q.2 Define cache memory? Explain the various mapping techniques associated with cache memories.
- Q.3 Describe in brief the data and control path techniques in pipelining.
- Q.4 With the help of a suitable block diagram, explain the architecture of 80×86 microprocessor.
- Q.5 Explain about DMA controller, with the help of a block diagram.
- Q.6 Give the difference between RISC and CISC processor. Describe in detail.

PART – C

- Q.1 Explain various instruction formats and illustrate the same with an example.
- Q.2 Write a short notes on the following -
- (a) Dynamic scheduling
 - (b) Memory segmentation
 - (c) Branch prediction
- Q.3 Explain how the instruction pipeline works. What are the various situation where an instruction pipeline stalls? Illustrate with an example.

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