310804

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B. Tech. III Sem. (Main) Exam., Dec. - 2019

Common for ECE/EIC

3EI4-04 Digital System Design

Time: 3 Hours **Maximum Marks: 120**

Instructions to Candidates:

Part – A: *Short answer questions (up to 25 words) 10 × 2 marks = 20 marks. All ten questions are compulsory.*

Part – B: *Analytical/Problem Solving questions 5 × 8 marks = 40 marks. Candidates have to answer five questions out of seven.*

Part – C: *Descriptive/Analytical/Problem Solving questions 4 × 15 marks = 60 marks. Candidates have to answer four questions out of five.*

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting materials is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART - A

Q.1 Evaluate the Boolean function $F = xy + \bar{x}z$ in a product of maxterms. [2]

Q.2 Draw the logic diagram for Boolean expression without simplifying [2]

$$F = (AB + \bar{A}\,\bar{B})(C\bar{D} + \bar{C}D)$$

Q.3 Show that dual of Ex – OR is equal to its complement. [2]

Q.4 Develop the K – map and solve the Boolean function [2]

$$F(x, y, z) = \sum (2, 3, 4, 5)$$

Q.5 Differentiate flip flop and Latch. [2]

Q.6 Mealy and Moore's machines can be differentiated on which factors? [2]

Q.7 Draw C – MOS inverter circuit. [2]

Q.8 Calculate noise margin for input voltage level 5V and threshold voltage level 4.15V. [2]

Q.9 Define number of transistor range for SSI, MSI, LSI and VLSI. [2]

Q.10 Define data type in VHDL. [2]

PART – B

Q.1 Convert the following numbers in required number system – [8]

(a) $[643]_{10} \rightarrow [\quad]_{\text{Excess-3}}$

(b) $[1010111]_{\text{GRAY}} \rightarrow [\quad]_2$

Q.2 Plot the logical expression $ABCD + A\bar{B}\bar{C}\bar{D} + A\bar{B}C + AB$ on a K – map; obtain the simplified expression from map. [8]

Q.3 Design a full subtractor and realize it with logic gates. [8]

Q.4 Construct a parallel binary adder with proper designing methodology. [8]

Q.5 Realize T flip – flop using S – R flip – flop. [8]

Q.6 Implement NOR gate using TTL. [8]

Q.7 Design a state diagram of a circuit to detect the sequence 1011. [8]

PART – C

Q.1 Analyze BCD to Excess – 3 code convertor. [15]

Q.2 How the Race – Round condition is raised? Give solution methodology for this problem. [15]

Q.3 Discuss Pseudo Random Binary sequence generator. [15]

Q.4 Write short note on FPGA. [15]

Q.5 Write VHDL code for MOD – 8 Asynchronous counter using structural modelling. [15]
