310704

Roll No. _____ Total No of Pages: 3

310704

B. Tech. III - Sem. (Main) Exam., February - 2021
Electronics & Communication Engineering
3EC4-04 Digital System Design
Common ECE/EIC

Time: 3 Hours **Maximum Marks: 120**

Instructions to Candidates:

Part – A: *Short answer questions (up to 25 words) 10 × 2 marks = 20 marks. All ten questions are compulsory.*

Part – B: *Analytical/Problem Solving questions (up to 100 words) 5 × 8 marks = 40 marks. Candidates have to answer five questions out of seven.*

Part – C: *Descriptive/Analytical/Problem Solving questions 4 × 15 marks = 60 marks. Candidates have to answer four questions out of six.*

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting materials is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART - A

Q.1 Draw symbol and truth table of all Logic gates. [2]

Q.2 What is Universal Logic Gate? Draw OR gate using NAND gate? [2]

Q.3 How is function of multiplexer different from de-multiplexer. [2]

Q.4 Define Hold – time and propagation delay time in Flip – Flops. [2]

Q.5 Write merit & demerits of ECL Logic family. [2]

Q.6 Compare Series and Parallel Adders. [2]

Q.7 What is difference between Synchronous and Ripple counter? [2]

Q.8 Write advantages and disadvantages of CMOS family. [2]

Q.9 Write briefly different modeling styles in VHDL. [2]

Q.10 What factors need to be optimized for a good VLSI design? [2]

PART – B

Q.1 Convert following number systems :

(a) Decimal to 8421 BCD code – 114, 37.2 [4]

(b) Convert to Hexadecimal – $(62.75)_8$ [4]

Q.2 Simply using K – Map, the following expression –

(a) $f(A, B, C, D) = \sum (0, 3, 6, 7, 9, 13, 14, 15)$ [4]

(b) $Y = \overline{A}BC + ABC + A\overline{B}\,\overline{C} + A\overline{B}C + ABC$ [4]

Q.3 Draw logic diagram of a 8:1 multiplexer and explain its working. [8]

Q.4 Write merits and demerits of various Logic families. [8]

Q.5 Briefly explain terms : Noise margin, Fan – in & fan – out, FPGA. [2×4=8]

Q.6 Draw a state diagram and logic diagram of 4 – bit ring counter using D Flip – Flops or JK Flip – Flop. [8]

Q.7 Why do we use VHDL? What is IC design flow? Explain briefly. [8]

PART – C

Q.1 (a) Using the Quine – McClusky method of tabular reduction minimize the function.

$f(A, B, C, D) = \sum m (0, 2, 3, 6, 7, 8, 9, 10, 13)$ [10]

(b) Simplify and implement by NAND gate: $Y = BD + BC\overline{D} + A\overline{BCD}$ [5]

Q.2 (a) Design a 4 – bit Binary to Gray code converter, also draw logic diagram. [10]

(b) Implement using 8 ×1 Mux the function - [5]

$f(A, B, C, D) = \sum m (1, 3, 4, 11, 12, 13, 14, 15)$

Q.3 (a) Convert J – K Flip – Flop into D and T Flip – Flop. [5]

(b) Design a Modulo – 10 counter using Flip – Flops. [5]

(c) Draw a ring counter using flip – flops and show state diagrams. [5]

[400]

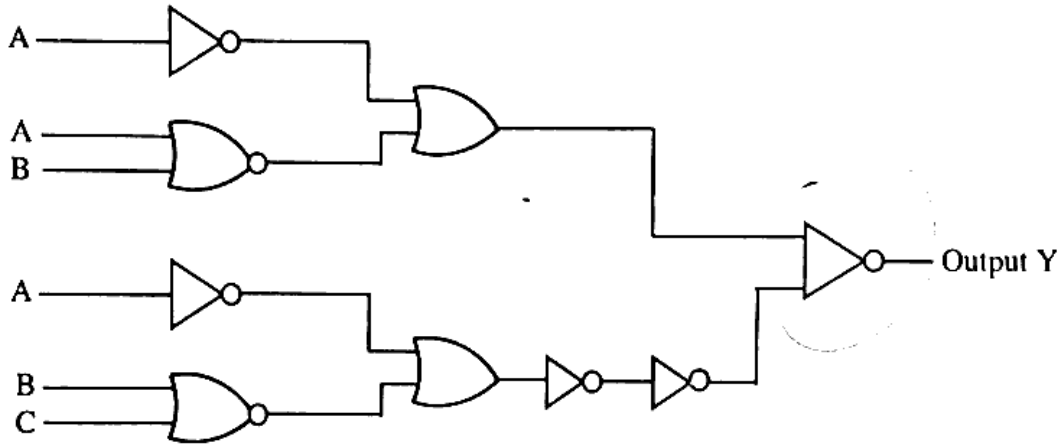
Q.4 (a) With diagram explain working of –

(i) CMOS NOR gate with two inputs [5]

(ii) MOS NAND gate with two inputs [5]

(b) Briefly describe interfacing issues of various logic families. [5]

Q.5 (a) Using universal logic gates draw a logic gate diagrams to implement the function of the following logic diagram. [5]



(b) What are sequential logic circuits? How they are designed using various flip – flop? Show the designing of a synchronous counter to count up and down with facility to skip any one number in counting sequence. [10]

Q.6 Describe the terms in context to VLSI design (any three)- [3×5=15]

(i) FSM and HDL

(ii) Data types and objects

(iii) VHDL constructs and codes

(iv) Behavioural and structural modeling