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31N0702

B.TECH. III SEM MAIN/BACK (NEW SCHEME)
ACADEMIC SESSION 2023-24
ELECTRONICS AND COMMUNICATION ENGINEERING

3EC4-02 - Digital Electronics

Common to EC, EI

Time : 3 Hours]

[Max. Marks : 70

[Min. Passing Marks :

Instructions to Candidates :

Part-A : Short Answer Type Questions (up to 25 words) 10 × 2 = 20 marks. All 10 questions are compulsory.

Part-B : Analytical/Problem Solving questions 5 × 4 = 20 marks. Candidates have to answer 5 questions out of 7.

Part-C : Descriptive/Analytical/Problem Solving questions 3 × 10 marks = 30 marks. Candidates have to answer 3 questions out of 5.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.

Use of the following supporting materials is permitted during examination. (Mentioned in form no. 205).

1_____ 2_____

Part–A

$10 \times 2 = 20$

Q. 1. Name any *two* self complimenting codes.

Q. 2. Prove AC + ABC = AC using Boolean algebra.

Q. 3. Convert of the following :

(i) $(1010011)_{Gray}$ to $(?)_{Binary}$

(ii) $(436)_{Decimal}$ to $(?)_{BCD}$

Q. 4. Reduce following function using K-map :

$$F(A, B, C) = \Sigma(0, 1, 2, 3, 5)$$

Q. 5. Which logical gates are known as universal gates and why ?

Q. 6. Draw logical circuit for full substractor.

Q. 7. Define fan in.

Q. 8. What is race-round condition ?

Q. 9. The Boolean expression $X = \overline{A} + \overline{B} + \overline{C}$ is logically equivalent to which single gate.

Q. 10. Draw NOR based S-R batch.

Part–B

$5 \times 4 = 20$

Q. 1. What is gray code ? Why it is important ?

Q. 2. State and prove associative and distributive theorems of Boolean algebra.

Q. 3. Solve using K-map :

$$F(A\ B\ C\ D) = \Sigma(0, 1, 3, 7, 9, 11) + d(4, 15)$$

Q. 4. Draw a multiplexer using only NAND gates which selects four inputs A_0 to A_3 using two select lines s_0 and s_1 ?

Q. 5. How do S-R, J-K and D flip flops differs ?

Q. 6. Compare the characteristics of different logic familier.

Q. 7. Discuss difference between combinational and sequential logic.

Part–C

3×10=30

Q. 1. Using the quine MC cluskey method and K-map method, obtain the minimal sum of product expression of the following function :

$$Y = \Sigma(0, 2, 3, 6, 7, 8, 10, 11, 12, 15)$$

Q. 2. Design 4 bit binary to gray code convertor.

Q. 3. Realize J-K flip flop using D flip-flop.

Q. 4. Write a brief note on interfacing of CMOS with TTL.

Q. 5. Design MOD-6 asynchronous counter using D flip-flops.

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