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Roll No. _____

31N0702

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B. Tech. III - Sem. (Main) Exam., May – 2023

Electronics and Communication Engineering

3EC4-02 Digital Electronics

Time: 3 Hours **Maximum Marks: 70**

Instructions to Candidates:

Part – A: *Short answer questions (up to 25 words) 10 × 2 marks = 20 marks. All **ten** questions are compulsory.*

Part – B: *Analytical/Problem solving questions 5 × 4 marks = 20 marks. Candidates have to answer **five** questions out of **seven**.*

Part – C: *Descriptive/Analytical/Problem Solving questions 3 × 10 marks = 30 marks. Candidates have to answer **three** questions out of **five**.*

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

Q.1 Find the equivalent gray code for $(478)_{10}$

Q.2 Covert the following -

(i) $(632.25)_8 \rightarrow (\ )_{10}$

(ii) $(2AC5.2B)_{16} \rightarrow (\ )_8$

Q.3 Differentiate between unipolar and bipolar logic family.

Q.4 Find the value of r, if -

$(54)_6 = (42)_r$

Q.5 Write the merits and demerits of ECL family.

Q.6 Find the minimum number of NAND gates required to realize $Y = A\bar{B}C$.

Q.7 Differentiate between Synchronous and Asynchronous counters.

Q.8 Explain the race-around condition in Flip-Flops.

Q.9 Convert $Y = A + B\bar{C} + A\bar{B} + A\bar{B}C$ into canonical form.

Q.10 *Define following -*

(a) Propagation Delay

(b) Fan in - Fan out

PART - B

Q.1 Minimize the following expression using k-map -

$Y = \sum m\,(1, 5, 6, 7, 11, 12, 13, 15)$

Q.2 Simplify the following function and implement it using NOR gate -

$F = A\bar{B} + ABD + AB\bar{D} + \bar{A}\bar{C}\bar{D} + \bar{A}B\bar{C}$

Q.3 Draw a neat circuit of TTL (Transistor Transistor Logic) NAND gate with totem pole output and explain.

Q.4 Design full Subtractor using 2:1 MUX. Also justify the truth table.

Q.5 Draw a state diagram and logic diagram of 4 bit Ring counter with D Flip-Flop.

Q.6 Explain the construction and working of Master Slave JK Flip-Flop.

Q.7 Write short notes on the following -

(a) VHDL

(b) Verilog

(c) FPGA

PART – C

Q.1 *Simplify the following function using Tabulation method and verify the result using k-map.*

$$F = \sum(0, 6, 9, 10, 13) + d(1, 3, 8)$$

Q.2 *Design a full Subtractor using half Subtractor.*

Q.3 (a) Construct a 4 bit serial adder using shift register and logic gates.

(b) Determine the next state for each of six unused states in the BCD ripple counter.

Q.4 (a) Covert the following -

(i) JK flip-flop to RS flip-flop

(ii) D flip-flop to JK flip-flop

(b) Draw the logic circuit for asynchronous mod-10 counter and draw its waveform.

Q.5 (a) Design a full adder using 4x 1 MUX

(b) Design a Excess-3 to BCD code converter using 4 bit adder.
