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M. Tech. I Sem. (Main) Exam., Dec. - 2018

VLSI Design

1MVL3 Digital System Design

Time: 3 Hours **Maximum Marks: 100**

Min. Passing Marks: 33

Instructions to Candidates:

*Attempt any **five questions.** Marks of questions are indicated against each question. Draw neat and comprehensive sketches wherever necessary to clearly illustrate your answer. Assume missing data suitable if any and specify the same. Use of following supporting material is permitted during examination. (Mentioned in form No. 205)*

1. NIL 2. NIL

Q.1 (a) Design a two input, two – output sequence detector which produces an output 1 every time the sequence 0101 is detected, and an output 0 at all other times. [10]

(b) What are the capabilities and limitations of finite state machines? [10]

Q.2 (a) Implement the following Boolean function by hazard – free OR – AND network.

$F = \sum (0, 2, 6, 7)$ [10]

(b) Find out minimal machines of M shown in table below: [10]

	N.S output	
P.S	**I1**	**I2**
A	D, 0	C, 1
B	E, 1	A, 1
C	H, 1	D, 1
D	D, 0	C, 1
E	B, 0	G, 1
F	H, 1	D, 1
G	A, 0	F, 1
H	C, 0	A, 1
I	G, 1	H, 1

Q.3 (a) Prove the De – Morgan theorem through expansion theorem. [10]

(b) Use the tabulation procedure to generate the set of prime implicants and to obtain all minimal expression for the following function: [10]

$F(v, w, x, y, z) = \sum (1, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 18, 19, 20, 21, 22, 23, 25, 26, 27)$

Q.4 (a) Prove that the NOR operation is functionally complete. [20]

(b) Define Reed - Muller equation.

(c) Determine the canonical product of sum form of

$T(x, y, z) = x' (y' + z)$

Q.5 (a) Design an asynchronous circuit which can be used in an automatic toll - collecting machine. Suppose the toll is 35 cents and the machine accepts nickels, dimes, and quarters. An electro – mechanical system, already available, accepts the coins sequentially (even if they are all dropped in simultaneously) and generates one of the three pulses x_5, x_{10}, or x_{25} whenever, a nickel, dime, or quarter, respectively, is accepted. The sequential circuit should produce a level output which would turn on a green light whenever the amount received by the machine is 35 cents or over. After a car has passed, a reset pulse x_r, is automatically produced, which turns the greens light off and reset the sequential circuit to its initial state. [10]

(b) Define the unate function and support the definition with example. [10]

Q.6 (a) The cell output of a typical cell of an iterative network is equal to 1, if and only if the input pattern of the preceding cells consists of groups of 0's and 1's, such that each group contains an odd number of members. [10]

(i) Construct a cell table.

(ii) Realize the typical cell using AND, OR, NOT logic.

(b) Differentiate CPLD and FPGA. Explain FPGA with suitable diagram. [10]

Q.7 (a) Implement following logic using a 4 × 3 PLA [10]

O1 = I1.I2 + I1`.I2` I3`. I4`

O2 = I1.I3` + I1`.I3.I4`+ I2

O3 = I1.I2 + I1.I3`+ I1`.12` .I4`

(b) Discuss the requirement that led to the design of the VHDL language, which of these requirements where a software language would fall short in describing hardware. [10]

Q.8 (a) Write VHDL code of 3 × 8 decoder in behavioral modeling style. [10]

(b) Implement Traffic Light controller using ASMs. [10]
